Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **1A**
2. **N.1Y**
3. **2A**
4. **N.2Y**
5. **3A**
6. **N.3Y**
7. **GND**
8. **N.4Y**
9. **4A**
10. **N.5Y**
11. **5A**
12. **N.6Y**
13. **6A**
14. **Vcc**

**.040”**

**.060”**

**1 14 13**

**2**

**3**

**4**

**5**

**12**

**11**

**10**

**9**

**6 7 8**

**MASK REF**

**ACT04A**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: GND**

**Mask Ref: ACT04A**

**APPROVED BY: DK DIE SIZE .040” X .060” DATE: 6/6/22**

**MFG: TEXAS INSTRUMENTS THICKNESS .025” P/N: 54ACT04**

**DG 10.1.2**

#### Rev B, 7/19/02